UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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17

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>05 August 2003</u> .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-24</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-24</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____ .

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth
> in section 102 of this title, if the differences between the subject matter sought to be patented and the
> prior art are such that the subject matter as a whole would have been obvious at the time the invention
> was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability
> shall not be negatived by the manner in which the invention was made.

2. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orimo et al.,

US Patent 5,630,135 in view of Valentaten et al., US Patent 5,250,940.

3. Referring to claim 1, Orimo et al. has taught a data processing system comprising:

(a) a plurality of processors for executing a series of different types of processings on

data to be processed (Orimo et al., figure 1 and column 3, lines 57-62) in a

prescribed order (Orimo column 8, lines 46-47), each processor executing a

processing different from one another and said data to be processed being image

data that consists of a plurality of pixel data (Orimo et al., abstract, column 10-,

lines 24-37, Graphic image data is comprised of pixel data.); and

(b) a memory for storing said data to be processed in association with state

information to represent the processing to be performed next for each pixel data

of said data to be processed, (Orimo et al., figure 5 and column 5, lines 1-12,

abstract, column 10-, lines 24-37,) wherein

(c) said processings are asynchronously executed on said data to be processed by said

plurality of processors, one processing is executed on each pixel data by one of

the processors at a time (Orimo et al., abstract, column 10, lines 24-37, column 2,

lines 9-16, The processors only rely on completion of a processing by the previous processor, not a clock signal, to determine when to execute the next processing).

4. Orimo et al. has not taught the plurality of processors sharing said memory. Valentaten et al. has taught a plurality of processors sharing a memory (Valentaten et al., Column 5, lines 56-65) in order to reduce bus bandwidth. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Orimo et al., have the plurality of processors share said memory, as taught by Valentaten et al., for the desirable purpose of reducing bus bandwidth (Valentaten et al., Column 5, lines 56-65).

5. Referring to claim 2, Orimo et al. has taught the data processing system wherein the plurality of processors each determine if said data to be processed can be processed based on said state information (Orimo et al., column 4, lines 4-9 and column 5, lines 27-39).

6. Referring to claim 3, Orimo et al. has taught the data processing system wherein the plurality of processors each execute a processing on said data to be processed, and then rewrite said state information corresponding to the processed data (Orimo et al., column 7, lines 54-56).

7. Referring to claim 4, Orimo et al. has taught the data processing system further comprising a first controller for controlling said plurality of processors to execute said series of processings based on said state information (Orimo et al., figure 1, element 100, column 4, lines 4-9 and column 5, lines 27-39, Each processor controls itself to execute

the processings based on state information and each individual control cooperates with
the control of the other processors to provide control for the entire system).

8. Referring to claim 5, Orimo et al. has taught the data processing system wherein the first
   controller rewrites said state information corresponding to processed data in response to
   the completion of each processing by said plurality of processors (Orimo et al., figure 1,
   element 100 and column 7, lines 54-56 Each processor controls itself to rewrite state
   information upon completion of each processing and each individual control cooperates
   with the control of the other processors to provide control for the entire system.).

9. Referring to claim 6, Orimo et al. has taught the data processing system further
   comprising a second controller for determining an attribute of said data to be processed
   (Orimo et al., column 5, lines 39-49), wherein said second controller rewrites said state
   information corresponding to said data to be processed in order to change the order of
   executing said series of processings if it is determined that said data to be processed has a
   prescribed attribute (Orimo et al., column 8, lines 46-66).

10. Referring to claim 7, Orimo et al. has taught the data processing system according to
    claim 6, wherein the second controller rewrites said state information corresponding to
    said data to be processed in order to remove a part of said series of processings, if it is
    determined that said data to be processed has a prescribed attribute (Orimo et al. column
    6, lines 16-43 where the process must be removed from the series of processings in order
    to execute.).

11. Referring to claim 8, Orimo et al. has taught the data processing system wherein said memory has one region to store said state information corresponding to a single region where data to be processed is stored (Orimo et al., figure 2, elements 201 and 205).

12. Referring to claim 9, Orimo et al. has taught the data processing system wherein said memory has one region to store said state information corresponding to a plurality of regions where data to be processed is stored (Orimo et al., figure 5, elements 3060 and 3063).

13. Referring to claim 10, Orimo et al. has taught the data processing system wherein said data to be processed is image data (Orimo et al., abstract, column 10-, lines 24-37, Graphic image data is processed.).

14. Claims 11-20 do not recite limitations above the claimed invention set forth in claims 1-10 and are therefore rejected for the same reasons set forth in the rejections of claims 1-10 above.

15. Referring to claim 21, Orimo et al. in combinatin with Valentaten et al., have taught the data processing system of claim 1, as described above, and further including wherein a given data item is stored at the same location in said memory after each of said plurality of processings is performed on said given data item (Valentaten et al., Column 5, lines 56-65, also see rejection to claim 1).

16. Referring to claim 22, Orimo in combination with Valentaten et al., have taught the data processing of claim 21, as described above, and wherein the state information for said given data item is stored at the same location in said memory after each of said plurality

of processings is performed on said given data item (Valentaten et al., Column 5, lines

56-65, also see rejection to claim 1).

17. Claim 23 and 24 do not recite limitations above the claimed invention set forth in claim

21 and 22 and are therefore rejected for the same reasons set forth in the rejection of

claims 21 and 22 above.

Response to Arguments

18. Applicant's arguments beginning at the last paragraph of page 12 and ending at the

bottom of page 13 have been considered but are moot in view of the new ground(s) of

rejection.

19. Applicant's arguments on pages 9-12 with respect to claims 1 and 11 have been

considered but they are not persuasive.

20. Applicant's arguments filed August 5, 2003 have been fully considered but they are not

persuasive.

21. On page 9, Applicant argues in essence:

"The prior art does not show, teach or suggest the invention as claimed in claim 1."

However, Orimo et al. in combination with Valentaten et al., which both qualify as prior

art, have taught the invention as claimed in claim 1 (See the rejection to claim 1 above.).

Therefore this argument is moot.

22. On pages 11-12, Applicant argues in essence:

*"Thus, Orimo et al. merely discloses that at least two of the processors 12 and 13 execute
different versions of the same program and thus execute the same type of processing.
Thus nothing in Orimo et al. shows, teaches or suggests that each processor executes
processing different from one another as claimed in claims 1 and 11. Rather, Orimo et
al. merely discloses executing different versions of the same program (i.e. same
processing)."*

However, Applicant is directed to column 1, lines 17-26, column 2, lines 21-25, column

3, lines 57-62, column 6, lines 54-63, column 7, lines 37-41, column 7, line 63-column 8,

lines 7, column 8, lines 46-57, and column 9, lines 6-9, column 10, lines 50-61, in Orimo

et al.. Orimo et al. has in fact taught multi-version processing whereby in one version an

event is processed having a low calculation precision and a short calculation time, and in

another version of the program the same event is processed with a high calculation

precision and a long calculation time. Low precision processing is a different type of

processing than high precision processing. Therefore, Orimo et al. has in fact taught

executing processings that are different from one another, i.e high and low precision

processing, as claimed in claim 1 and 11. Therefore this argument is moot.

23. On page 12, Applicant argues in essence:

*"Additionally, Orimo et al. merely discloses that the processors 12 and 13 process the
same data simultaneously (col. 8, lines 34-37, col. 10, lines 11-13). However, as claimed
in claims 1 and 11, one processing is executed on each pixel data by one processor at a
time. However, Orimo et al. teaches away from the claimed invention and processes the
data simultaneously in processors 12 and 13."*

However, Orimo et al. have taught that one processing is executed on each pixel data by

one processor at a time. Orimo et al. have taught executing one version of program in

one processor i.e. one processing is executed on a pixel data at a time (Orimo et al.,

column 3, lines 57-62), and executing another version of the program in a second

processor, i.e. a second processing is executed on a pixel data at the same time (Orimo et

al., column 3, lines 57-62). The extent to which Applicant has claimed the invention,

Orimo et al. in Combination with Valentaten et al. still reads on the claims. Therefore

this argument is moot.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this

    Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

    § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

    CFR 1.136(a).

25. A shortened statutory period for reply to this final action is set to expire THREE

    MONTHS from the mailing date of this action. In the event a first reply is filed within

    TWO MONTHS of the mailing date of this final action and the advisory action is not

    mailed until after the end of the THREE-MONTH shortened statutory period, then the

    shortened statutory period will expire on the date the advisory action is mailed, and any

    extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

    advisory action. In no event, however, will the statutory period for reply expire later than

    SIX MONTHS from the date of this final action.

26. Any inquiry concerning this communication or earlier communications from the

    examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-

    3993. The examiner can normally be reached on Monday-Friday, 9-6:30.

27. If attempts to reach the examiner by telephone are unsuccessful, the examiner's

    supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone numbers for

    the organization where this application or proceeding is assigned are (703) 746-7239 for

    regular communications and (703) 746-7238 for After Final communications.

28. Any inquiry of a general nature or relating to the status of this application or proceeding

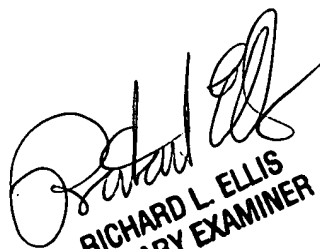   should be directed to the receptionist whose telephone number is (703) 305-3900.

tlm
October 3, 2003

RICHARD L. ELLIS
PRIMARY EXAMINER